

CLAIMS

What is claimed is:

1. A microelectronic structure comprising:
a substrate comprising circuits;
a plurality of conductive bumps provided in adjacent relationship to each other on said substrate in electrical contact with said circuits, each of said plurality of conductive bumps having an upper surface, a pair of sidewalls, an outer wall and an inner wall; and
a conductive layer provided on each of said plurality of conductive bumps, wherein said conductive layer is absent from at least one of said sidewalls.
2. The microelectronic structure of claim 1 wherein said conductive layer is absent from both of said pair of sidewalls.
3. The microelectronic structure of claim 1 further comprising at least one shoulder provided in said conductive layer at said upper surface.

4. The microelectronic structure of claim 3 wherein said conductive layer is absent from both of said pair of sidewalls and wherein said at least one shoulder comprises a pair of shoulders.

5. The microelectronic structure of claim 1 wherein said conductive layer is absent from said inner wall.

6. The microelectronic structure of claim 5 wherein said conductive layer is absent from both of said pair of sidewalls.

7. The microelectronic structure of claim 5 further comprising at least one shoulder provided in said conductive layer at said upper surface.

8. The microelectronic structure of claim 7 wherein said conductive layer is absent from both of said pair of sidewalls and wherein said at least one shoulder comprises a pair of shoulders.

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9. The microelectronic structure of claim 1 wherein said conductive layer is formed of a conductive metal selected from the group consisting of Au, Ag, Pt, Pd, Al, Cu, Sn and alloys thereof.

10. The microelectronic structure of claim 9 wherein said conductive layer is absent from both of said pair of sidewalls.

11. The microelectronic structure of claim 9 further comprising at least one shoulder provided in said conductive layer at said upper surface.

12. The microelectronic structure of claim 11 wherein said at least one shoulder comprises a pair of shoulders.

13. A microelectronic structure comprising:
a substrate comprising circuits; /
a plurality of conductive bumps provided in adjacent relationship to each other in rows on said substrate and in electrical contact with said circuits, each of said plurality of conductive bumps having an upper surface, a pair of sidewalls, an outer wall and an inner wall;

a conductive layer provided on each of said plurality of conductive bumps, wherein said conductive layer is absent from at least one of said sidewalls; and

a protection layer provided on said substrate adjacent to said rows of said plurality of conductive bumps.

14. The microelectronic structure of claim 13 wherein said conductive layer is absent from both of said pair of sidewalls.

15. The microelectronic structure of claim 13 wherein said conductive layer is absent from said inner wall.

16. The microelectronic structure of claim 13 further comprising a test probe pad provided on said substrate adjacent to each of said plurality of conductive bumps and in electrical contact with said conductive layer.

17. A method of fabricating a conductive bump on a substrate, comprising the steps of:

providing a substrate comprising circuits;

providing a bump-forming structure having an upper surface, a pair of sidewalls, an outer wall and an inner wall on said substrate in electrical contact with said circuits;

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providing a conductive layer on said bump-forming structure; and

removing said conductive layer from at least one of said sidewalls.

18. The method of claim 17 further comprising the step of removing said conductive layer from both of said sidewalls.

19. The method of claim 17 further comprising the step of removing said conductive layer from said outer wall.

20. The method of claim 17 further comprising the step of providing at least one shoulder in said conductive layer at said upper surface.